IN THE CLAIMS

Please Amend Claims 1, 3, 40, 43, 45 and 49 as follows:

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method to conserve power comprising:

in a digital signal processor integrated circuit including an internal memory, a reduced instruction set computing (RISC) processor and one or more digital signal processing (DSP) units,

selectively swapping activity between the RISC processor and the one or more DSP units to conserver power;

selectively stopping a clocking of a respective one of the one or more DSP units; and

selectively activating one of a plurality of memory clusters in the internal memory and maintaining ~~a state of~~ all other memory clusters of the plurality of memory clusters in the internal memory in a stable state.

2. (Previously Presented) The method of claim 1, wherein

the selective swapping of activity from the RISC processor to the one or more DSP units includes

inactivating bus drivers on data paths in the RISC processor and activating bus drivers on data paths in the one or more DSP units.

3. (Currently Amended) The method of claim 1, wherein

selectively activating one of a plurality of memory clusters in the internal memory and maintaining ~~a state of~~ all other memory clusters in a stable state includes

selecting a data flow path between the one activated memory cluster, the RISC processor, and the one or more swapped DSP units ~~to change state~~, and

maintaining a stable state on data flow paths between inactivated memory

clusters, the RISC processor, and the one or more DSP units.

4. (Previously Presented) The method of claim 1, wherein

the selective stopping of the clocking of the one or more DSP units is responsive to the respective one or more DSP units being inactive.

5. (Previously Presented) The method of claim 1, wherein

the selective stopping of the clocking of the one or more DSP units is responsive to the respective one or more DSP units not executing an instruction.

6. (Previously Presented) The method of claim 1, wherein

the selective activating of one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

7-39. (Cancelled)

40. (Currently Amended) The method of claim 2, wherein

selectively activating one of a plurality of memory clusters in the internal memory and maintaining ~~a state of~~ all other memory clusters in a stable state includes

selecting a data flow path between the activated memory cluster, the RISC processor, and the one or more DSP units to change state, and

maintaining a stable state on data flow paths between inactivated memory clusters, the RISC processor, and the one or more DSP units.

41. (Previously Presented) The method of claim 40, wherein

the selective stopping of the clocking of one or more DSP units is respectively responsive to those one or more DSP units not executing an instruction.

42. (Previously Presented) The method of claim 40, wherein

the selective activating of one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

43. (Currently Amended) A method to conserve power in a digital signal processor integrated circuit, the method comprising:

in an integrated circuit

selectively swapping activity between a reduced instruction set computing (RISC) processor and a plurality of digital signal processing (DSP) units to conserver power;

selectively stopping the clocking of at least one of the plurality of DSP units; and

selectively activating one of a plurality of memory clusters in an internal memory coupled to the plurality of DSP units and maintaining ~~a state of~~ other memory clusters in the internal memory in a stable state.

44. (Previously Presented) The method of claim 43, wherein

the selective swapping of activity from the RISC processor to the plurality of DSP units includes

inactivating bus drivers on data paths in the RISC processor and activating bus drivers on data paths in one or more of the plurality of DSP units.

45. (Currently Amended) The method of claim 43, wherein

selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters includes

selecting a data flow path between the activated memory cluster, the RISC processor, and the plurality of DSP units, the selected data flow path to change state, and

maintaining a stable state on data flow paths between inactivated memory clusters, the RISC processor, and the plurality of DSP units.

46. (Previously Presented) The method of claim 43, wherein

the selective stopping of the clocking of the at least one of the plurality of DSP units is respectively responsive to the at least one of the plurality of DSP units being inactive.

47. (Previously Presented) The method of claim 43, wherein

the selective stopping of the clocking of the at least one of the plurality of DSP units is respectively responsive to the at least one of the plurality of DSP units not executing an instruction.

48. (Previously Presented) The method of claim 43, wherein

the selective activating of one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

49. (Currently Amended) A method to conserve power in a digital signal processor integrated circuit, the method comprising:

in an integrated circuit

selectively swapping activity between a reduced instruction set computing (RISC) processor and a plurality of digital signal processing (DSP) units, including activating and inactivating bus drivers on data paths in the RISC processor and the plurality of DSP units to conserver power;

selectively stopping the clocking of at least one of the plurality of DSP units;

selectively activating one of a plurality of memory clusters in an internal memory and maintaining ~~a state of~~ other memory clusters in the internal memory in a stable state, including selecting a data flow path between the activated memory cluster, the RISC processor, and the plurality of DSP units, the selected data flow path to change state; and

maintaining a stable state on data flow paths between inactivated memory clusters, the RISC processor, and the plurality of DSP units.

50. (Previously presented) The method of claim 49, wherein

the selective stopping of the clocking of the at least one of the plurality of DSP units is responsive to the at least one of the plurality of DSP units not executing an instruction.

51. (Previously presented) The method of claim 49, wherein

the selective activating of one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

52. (Previously presented) The method of claim 2, wherein
the selective swapping of activity from the one or more DSP units to the RISC processor includes
activating bus drivers on data paths in the RISC processor and inactivating bus drivers on data paths in the one or more DSP units.

53. (Previously presented) The method of claim 44, wherein
the selective swapping of activity from the plurality of DSP units to the RISC processor includes
activating bus drivers on data paths in the RISC processor and inactivating bus drivers on data paths in the plurality of DSP units.

54. (Previously presented) The method of claim 49, wherein
the selective swapping of activity from the RISC processor to the plurality of DSP units includes
inactivating bus drivers on data paths in the RISC processor and activating bus drivers on data paths in the plurality of DSP units.

55. (Previously presented) The method of claim 49, wherein
the selective swapping of activity from the plurality of DSP units to the RISC processor includes
activating bus drivers on data paths in the RISC processor and inactivating bus drivers on data paths in the plurality of DSP units.